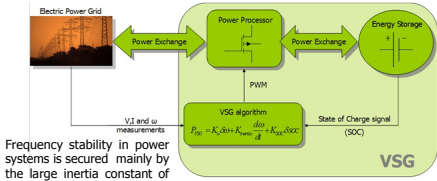


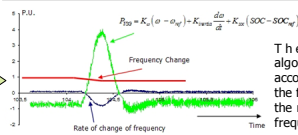
# Testing a Virtual Synchronous Generator in a Real-Time Simulated Power System

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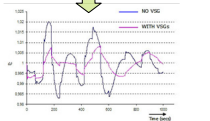
## The VSG Concept



Frequency stability in power systems is secured mainly by the large inertia constant of synchronous machines which, due to its counteracting nature, smooths out the various disturbances. The increasing growth of small scale dispersed generation will cause this inertia constant to decrease having as a result an instable power system. A promising solution to such a development of events is the Virtual Synchronous Generator (VSG) where three distinctive components, namely a power converter an energy storage device and the appropriate control algorithm, are brought together to replace the lost inertia.



The VSG control algorithm controls power according to the value of the frequency of the grid, the rate of change of the frequency and the SOC.



The VSG action counteracts the large frequency deviations, caused mainly by load variations, and decreases them in size.

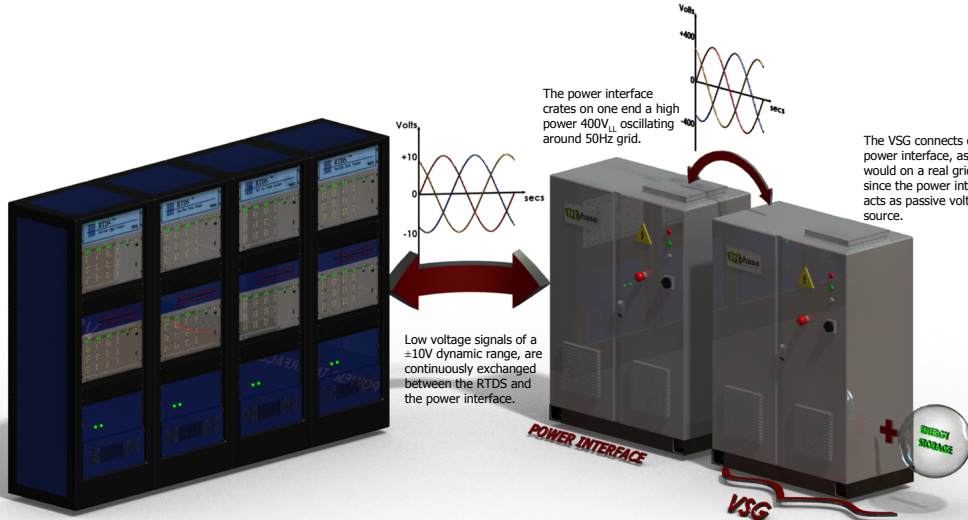
## THE VSYNC PROJECT

Virtual Synchronous Machines For Frequency Stabilisation In Future Grids With A Significant Share Of Decentralized Generation.

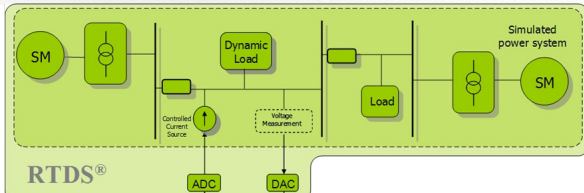
- Duration: 3 years (Oct 2007 till Oct 2010)
  - Budget: € 3.25 million
  - Coordinator: ECN, The Netherlands
  - Project manager: Dr. K. Visscher, [visscher@ecn.nl](mailto:visscher@ecn.nl)
- Participating institutions: ECN, TU/e, TU Delft, LEUVEN, labelin, and others.

## Acknowledgements:

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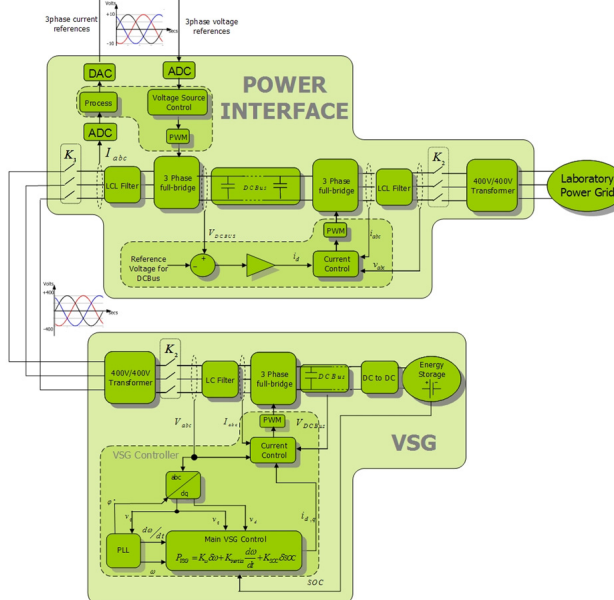
The RTDS simulates a specified power system in real-time where frequency disturbances occur by a dynamic load that varies between 0% and 7% of the total power generated by the Synchronous Machines (SM).



The power interface uses the Laboratory power grid to amplify the reference signals from the RTDS so that a 3 phase 400V 50Hz grid can be created for the VSG to be connected to. Therefore the power interface accommodates two '3-phase full bridges' that share the same DC bus.

The '3-phase full bridge' of the power interface that is connected to the VSG acts as a voltage source, meaning that it has a passive behavior when it comes to power exchange as well as having the voltage dynamics of the simulation. That allows the VSG to dictate how much power is pushed to or absorbed from the simulated power system, according to the disturbance.

When the VSG action occurs though, power is actually extracted from as well as pushed in to Laboratory power grid. This is achieved by setting '3-phase full bridge' of the power interface that is connected to the Laboratory power grid to act as a voltage regulator for the DC bus.



A VSG algorithm has been developed on MatLab/Simulink to run exclusively on the Triphase® inverter system through a dedicated FPGA interface developed by Triphase®. In order to test the hardware implemented VSG and study its effects within a power system, it is interfaced with a real-time digital simulator from RTDS® where real time simulation of power systems is made possible through a parallel processing architecture.

The RTDS® is often used in closed loop testing with real external hardware because of the Analogue to Digital and Digital to Analogue Converters (ADC, DAC) it is equipped with. Keeping in mind that these ADCs and DACs have a dynamic range of ±10V max rated at 5mA max and the Triphase® inverter system is rated at 16kVA it is clear that a power interface has to come in between to make this union possible.

The purpose of this power interface is to come in between the VSG and the RTDS. That is because, the analogue I/Os of the RTDS have a dynamic range of ±10V max rated at 5mA max and the VSG is rated at 16kVA. The power interface accommodates components to handle the VSGs high power requirements as well as analogue I/Os matching those of the RTDS.

Three analogue signals carrying the voltage dynamics information of the three-phase simulated power system are continuously sent from the DACs of the RTDS® to the ADCs of the power amplifier and the latter amplifies those signals to the appropriate level using power from the laboratory's power grid. Hence the power interface in effect creates a three phase power grid that has the dynamics of the simulated power system. To close the loop, current information is sent back to the RTDS®, this time though the signals are sent from the DACs of the power amplifier to the ADCs of the RTDS® and like that the simulation is updated with the action of the VSG.